INTERFACE BETWEEN IBM 1800 AND PHASED ARRAY ANTENNA

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by

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Certificate

This is to certify that the thesis entitled 'Interface between IBM 1800 and Phased Array Antenna' is a record of the work carried out under our supervision and that it has not been submitted elsewhere for a degree.

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S Y N O P S I S

A scheme is proposed for the interface between the Computer (IBM 1800) and phase shifters of a 256 element phased array antenna. The design is implemented with RTL gates and flip-flops for a 16 element array. The 16 element interface allows Sequential and Random Loading of the phase shifter registers. Design considerations for extension of the interface for larger arrays are discussed.

CHAPTER I

INTRODUCTION

In recent years the growing need for radars to provide longer detection ranges and faster data rates (short reaction times) and accomodate increased target densities has resulted in new approach to radar design. Most promising of these approaches is electronic scanning. With electronic scanning, it is possible to obtain practically instantaneous slewing of an antenna beam to any position in a designated sector. Electronic scanning is defined as a method of positioning an electromagnetic beam in space by electronic means with the antenna apperture remaining fixed in space and no mechanical mechanism involved in the scanning process.

Electronic scanning radars are characterized by increased apperture size, greater radiating power from thousands of radiating elements, faster data rates (reaction times) because of inertialess scanning and increased multimode operation. The three basic electronic scanning techniques are phase (real time, a special case), frequency and electronic feed switching. In a phase scanning system the beam is positioned electronically by adjusting the differential phase between elements of an array in a predetermined manner. A unique beam position corresponds to a

progressive phase shift setting in the network feeding the array. Many phased arrays are designed to use digital or digitized phase shifters in which the phase shift varies in discete steps rather than continuously. Most of the phased array applications require narrow beam and hence many elements. This gives the first problem: how to feed 10^3, 10^4 or 10^5 elements?

The electronically controlled phased array radar antenna has received considerable attention in the last decade. Requiring no mechanical motion for steering, it can scan in microseconds or with some phase control elements in nanoseconds; even multiple beams can be formed electronically. In future, for almost every antenna steering application the electronically steered array will be desired provided cost, reliability, power handling capability, band width and insertion losses can be made comparable with the mechanical system. At present, only the electronic array can be used to achieve microsecond steering. Using an electronic scanning radar to perform several functions with a beam that can be positioned in microseconds necessitate digital computer control and most electronic scanning radar systems are particularly well adopted and designed for such control.

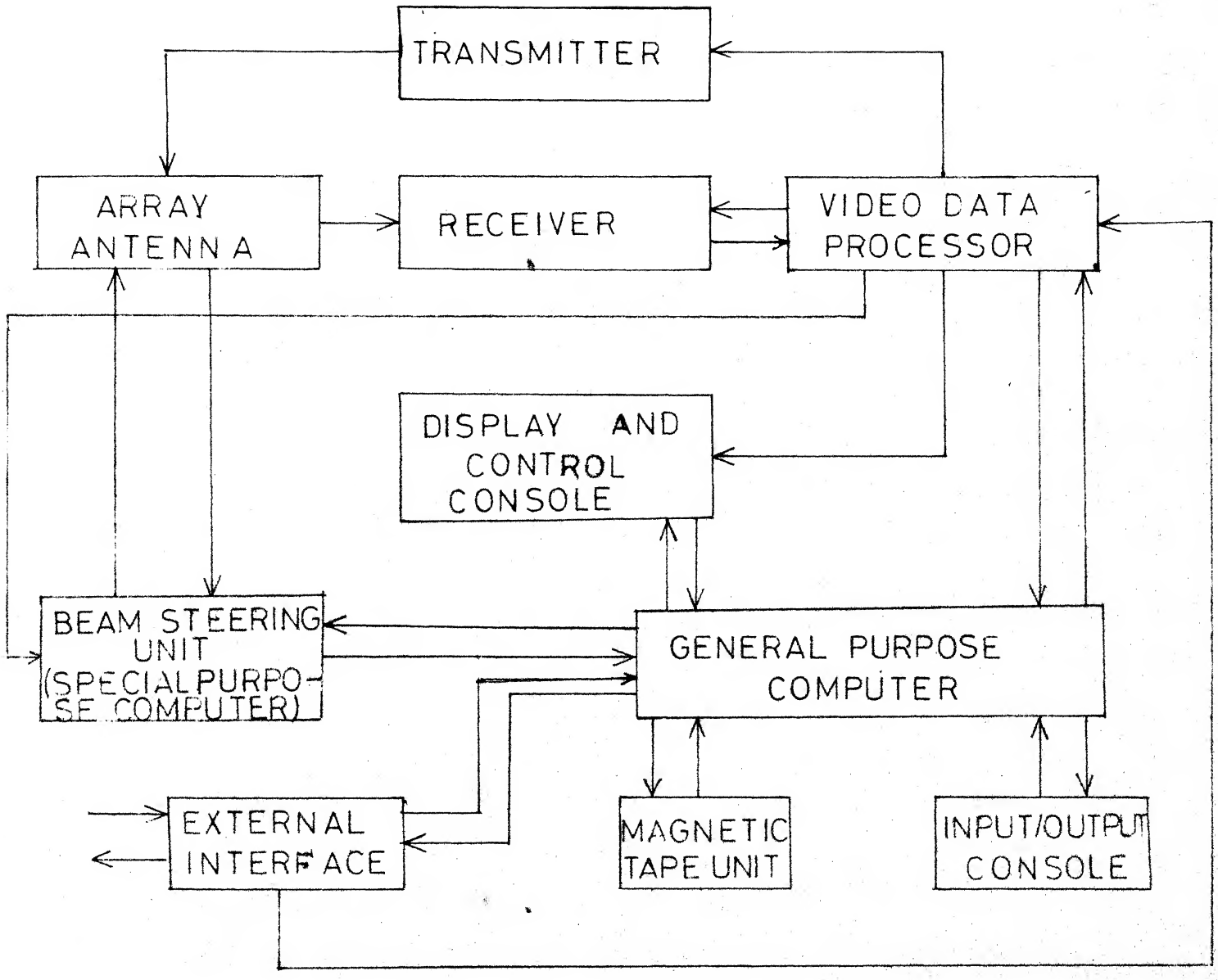

FIG. 1-1 FUNCTIONAL BLOCK DIAGRAM OF ELECTRONIC SCANNING RADAR SYSTEM.

A generalized functional block diagram of electronic scanning radar system is given in Figure 1.1. The main subsystems are

(1) Array antenna

(2) Beam Steering unit (Special purpose Computer)

(3) Transmitter

(4) Receiver

(5) General purpose computer

(6) Input/Output interface

(7) Control console and displays

The beam steering unit includes computer controlled self checking equipment to permit detection and reporting of equipment failures to the system computer.

The prime requirements for steering a phased array antenna is the generation of the appropriate phase values for all elements within the array. A special purpose computer referred to as the beam steering computer (BSC), is commonly used to generate these phase values after receiving prime steering data from an external source such as a general purpose computer. The general purpose computer transfers two basic steering commands which permit the positioning of the beam in two dimensions. Typically these two commands consist of the new values of angles in the basic azimuthal

and elevation direction. Having received the data in the form of phase differences between adjacent rows or columns, it is the function of the BSC to multiply by all integers upto the maximum number of rows or columns and then sum the appropriate values to determine the actual phase for each element in the array. The time required for computation is usually dictated by the overall system requirements while the equipment complexity must be minimized in the interest of cost, weight and reliability.

The interface, between the BSC and the phased array consists of two sections of element registers. These consist of a shift register for each element. As the first section is being conditioned, the second section is commanding all of the array elements to the previous pointing angle. When a new angle command is to be executed, the contents of the first section of the buffer are jammed into the second section of the buffer.

The scope of the project is to design a scheme for the interface for transfering 64 words of 16 bits each to the phase shifters of 256 element array and to fabricate an experimental hardware for 4 words transfer.

CHAPTER II

SYSTEM DESIGN FOR THE INTERFACE FOR 256 ELEMENT ARRAY

It is required to design an interface between the the IBM 1800 data acquisition and control system and the phase shifters of the 256 element array. Data to be transferred is four bits per phase shifter element. The digital and analog output (DAO) feature of IBM 1800 provides register output by means of which digital information is transferred from core storage to the sixteen bit output registers. The loading of a 16-bit output register is signalled (indicated) by a 'Data Ready Pulse' which comes from the processor-controller. The data transfer to the external custumer device can be under data channel operation or direct program control. In data channel operation the data transfer is initiated by an XIO instruction where as in direct program control every data word transfer requires the execution of an XIO instruction. In direct program control execution of each XIO requires about 10 to 12 microseconds. In data channel operation the speed can be improved.

Timing considerations:

A typical requirement of a phased array radar is 1000 beam positions per second allowing 1 millisecond in each beam position. For a phased array Radar of 256 elements with 4 bits per phase shifter, 64, 16-bit word transfers are required. If output is under a data channel it takes (64x4) 256* microseconds for this transfer which is well with in the limits of the requirements. Even in direct program control operation it takes 710@ microseconds which is also within the requirements.

It is proposed to take the output of two digital output registers of IBM 1800 system one of them being used as 'Control Register' and the other as the 'Data Register'. The interface facilitates the loading of the array in two modes namely sequential and random. In the sequential loading phase shifters are loaded sequentially and the phase shift for all elements have to be supplied. In the random loading, only those phase shifters that are selected by the 'Control Register' are loaded. Random loading is desirable in cases where only a few phase shifters need updating to steer the beam into new position. The functional block diagram of the scheme proposed

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* In data Channel operation it takes 4 microseconds (minimum) for each data word transfer.

@ In direct program control it takes about 11 microseconds for each data word transfer.

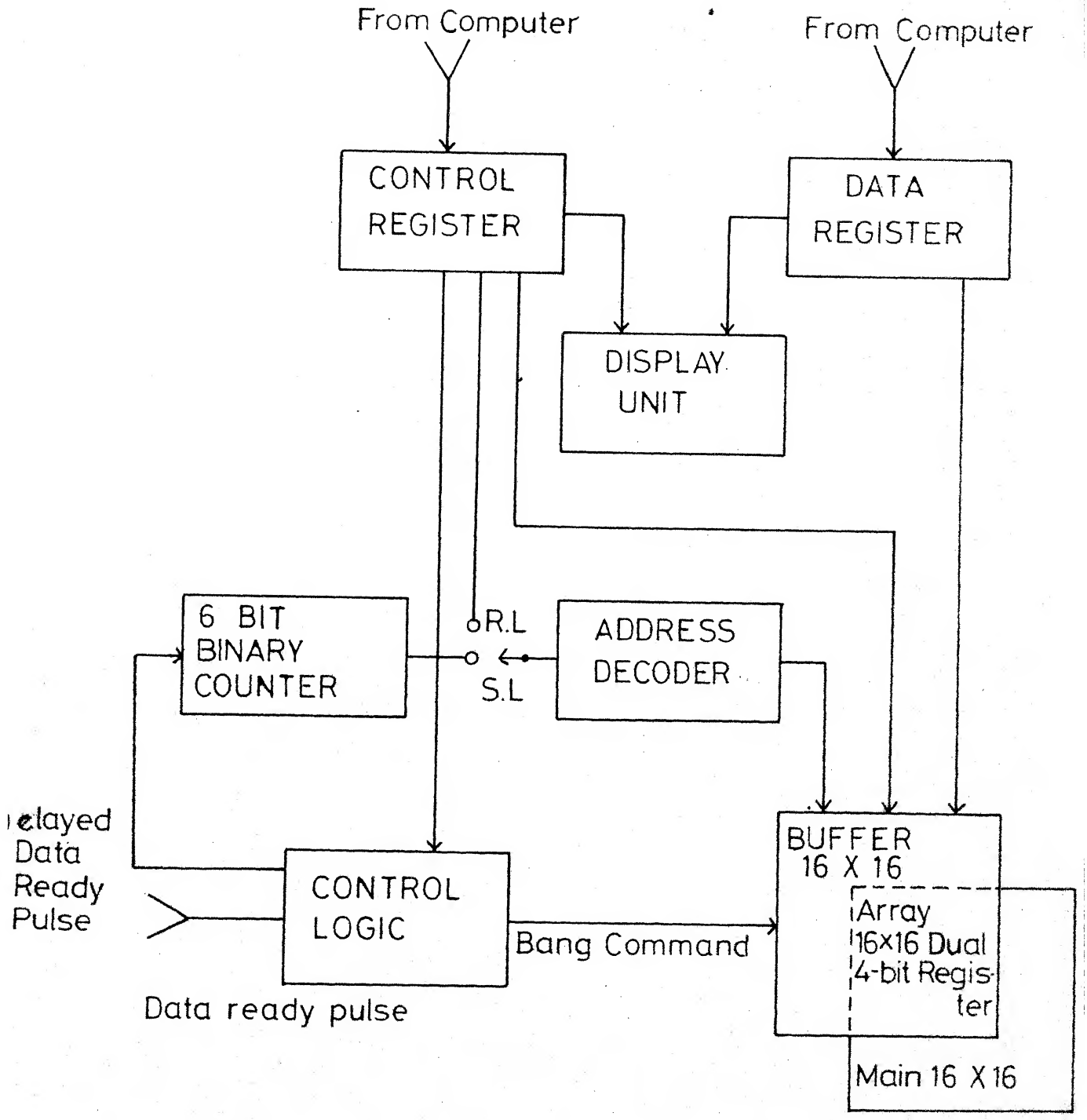


FIG.2-1. Functional block diagram of the interface.
S.L. Sequential loading.
R.L. Randam loading.

for the interface is shown in Figure 2-1.

Array of Element Registers:

In a phased array antenna the beam position depends upon the digital data fed to the (256 in this case) phase shifters of the array each of which requires 4 bit data. To steer the beam into a new position 256 x 4 new data bits must all be loaded simultaneously. Since computer supplies 16 bits a time it is necessary to accumulate 64 words into a buffer before applying the same to the phase shifters. If the buffer is not provided and the phase shifters are loaded directly with the new phase commands then the beam takes undesired positions before it attains the new position unless the transmission is stopped during the loading phase. Suspension of transmission reduces the time for which the area can be used to operate the radar. Hence the buffer is provided so that it can be loaded sequentially withoutdisturbing the settings of the phase shifters which command the beam to the previous pointing angle. When all the buffers are completely loaded with the new phase commands, the information from the buffer is transferred to the phase shifters so that the beam is steered to the new position.

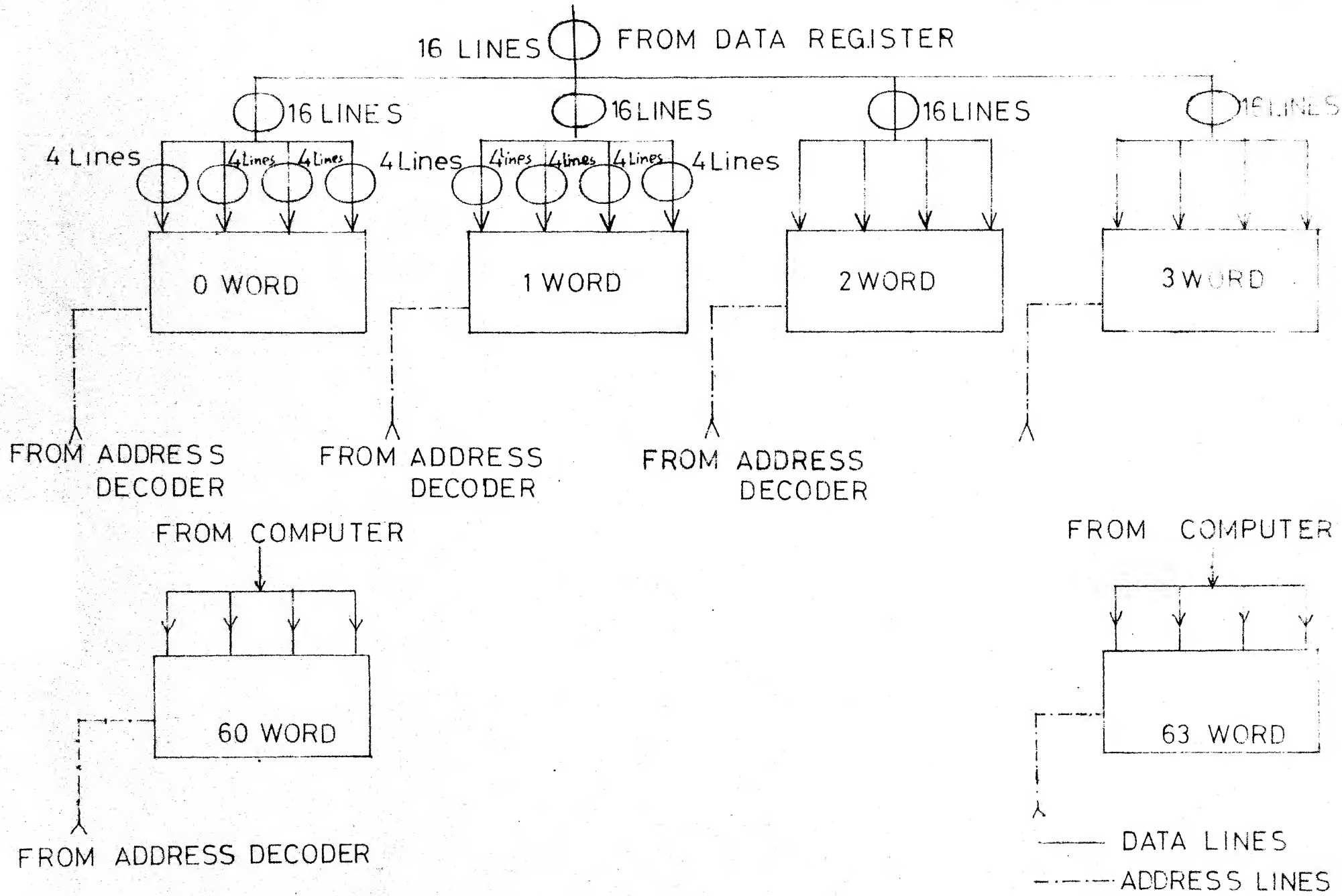


FIG. 2-2(a) ARRAY DETAILS

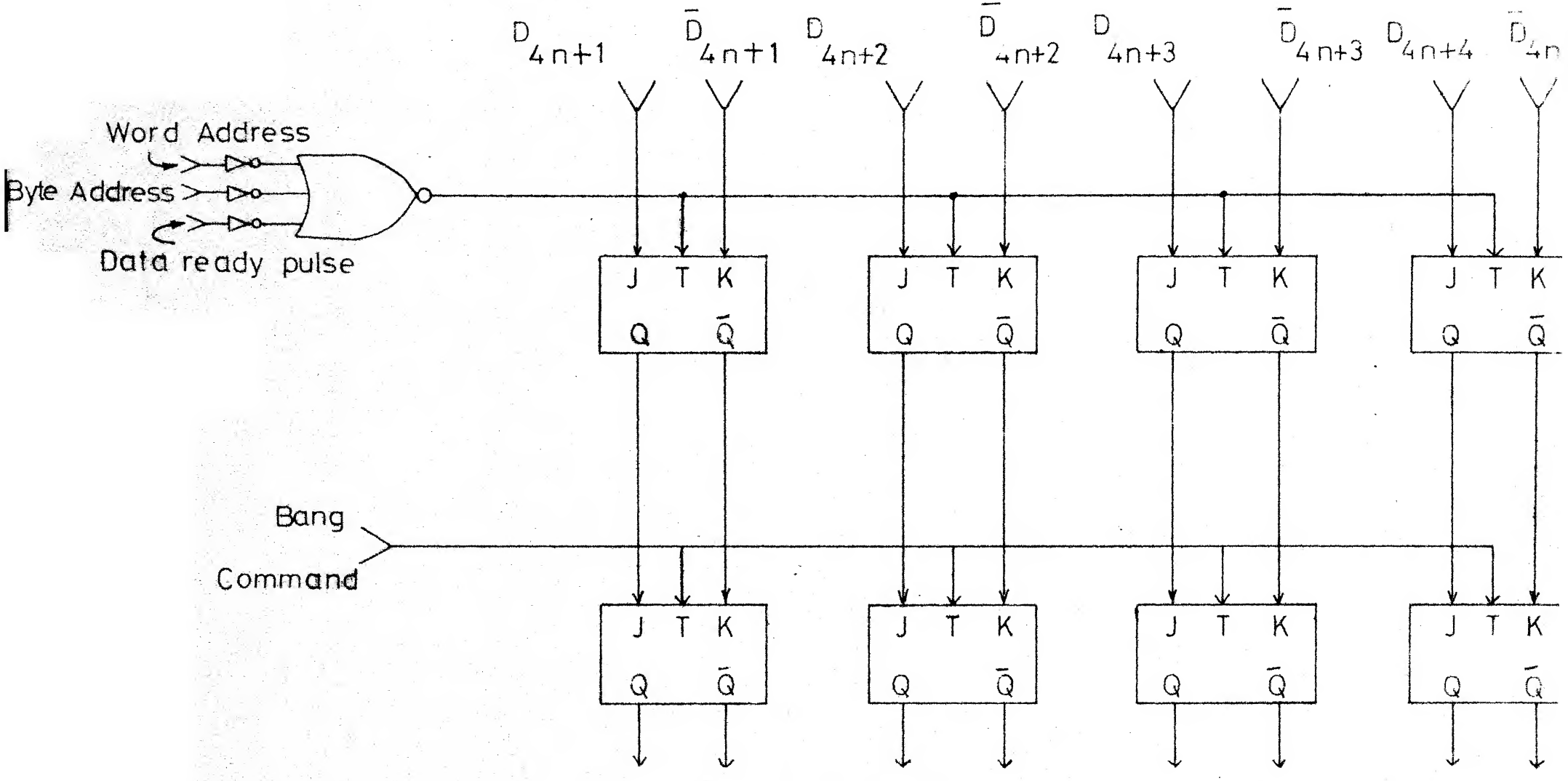
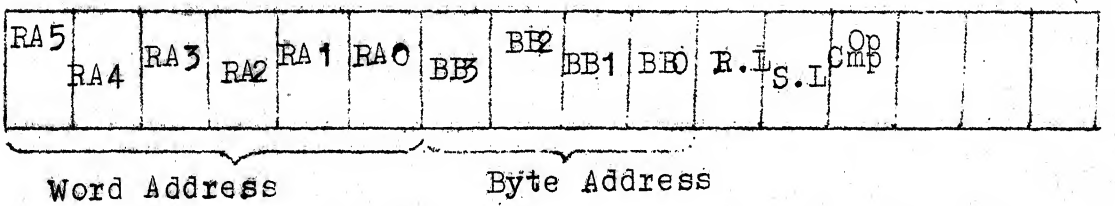


FIG. 2-2 (b) DUAL 4 BIT SHIFT REGISTER n = 0 ····· 63

Therefore an array of 16 x 16 dual 4 bit shift registers is employed. The array details are shown in Figure 2.2. The Buffer section of the dual 4-bit registers is loaded serially. On completion of serial loading the contents of the Buffer section are all transferred to the phase shifters with a single pulse referred to as 'Bang Commad'.

Control and Data Registers:

The 'Control Register' sets the mode of operation (sequential or random) and enables the array to accept data which comes from the 'Data Register'. The format of the 'Control Register' is given below in Figure 2.3(a).



Op Comp = Operation Complete

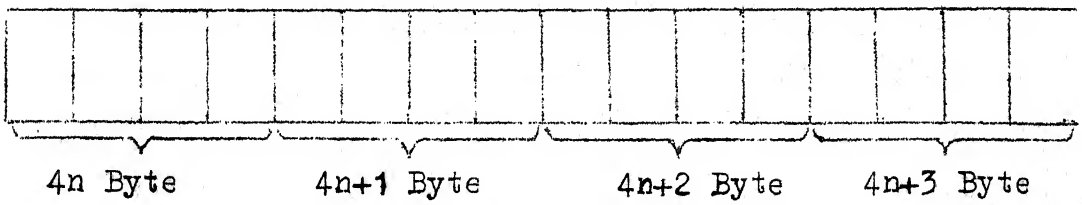
R.L. = 0 S.L = 1 enables Random Loading

R.L. = I S.L = 0 enables Sequential Loading

Operation complete = 0 enables Bang Command.

Figure 2.3(a) Format of the 'Control Register'

The 'Data Register' contains the information to be transferred to the phase shifters (shown below in Figure 2.3(b)). In conjunction with the data from the 'Control Register' the 'Control Logic' directs the data into appropriate register of the array.

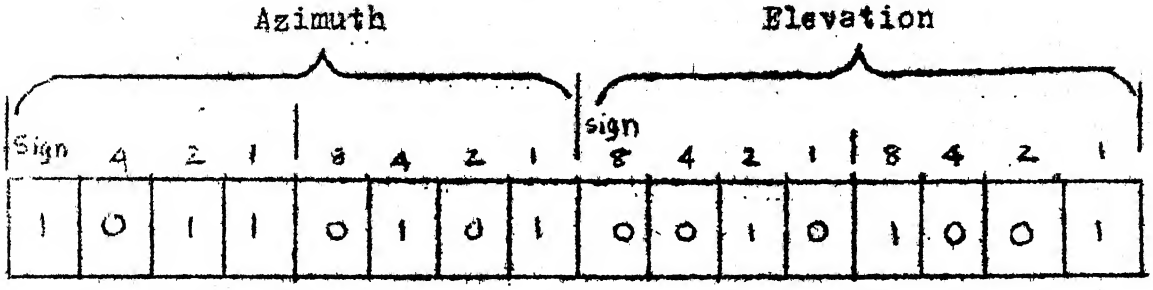


N = 0 ... 63

Figure 2.3(b) Data Register Format.

After transferring 64 words into the 'Data Register' azimuth and elevation in BCD form are loaded into the 'Data Register' and partially into the 'Control Register'. The ' Op-Complete' bit of the control register when turned off enables the 'Control Logic' to execute 'Bang Command'. The zero status of the ' Op-Complete' bit is also employed to enable the display of azimuth and angle

of elevation. Typical values of azimuth and elevation lie between ± 45°. To code the two angles in BCD form with sign bits 16 bits are required. So 16 bits of the 'Data Register' are used for this purpose. The format is shown below in Figure 2.4 . The 'Data Register' is shown to contain azimuth of + 35° and elevation of -29°.



Data Register Containing Azimuth and Elevation in BCD form

Sign 1 = Poseitive 0 = Negative } Azimuth in BCD

0 to 7 of Data Register }

8 to 15 of Data Register : Elevation in BCD

FIGURE 2.4

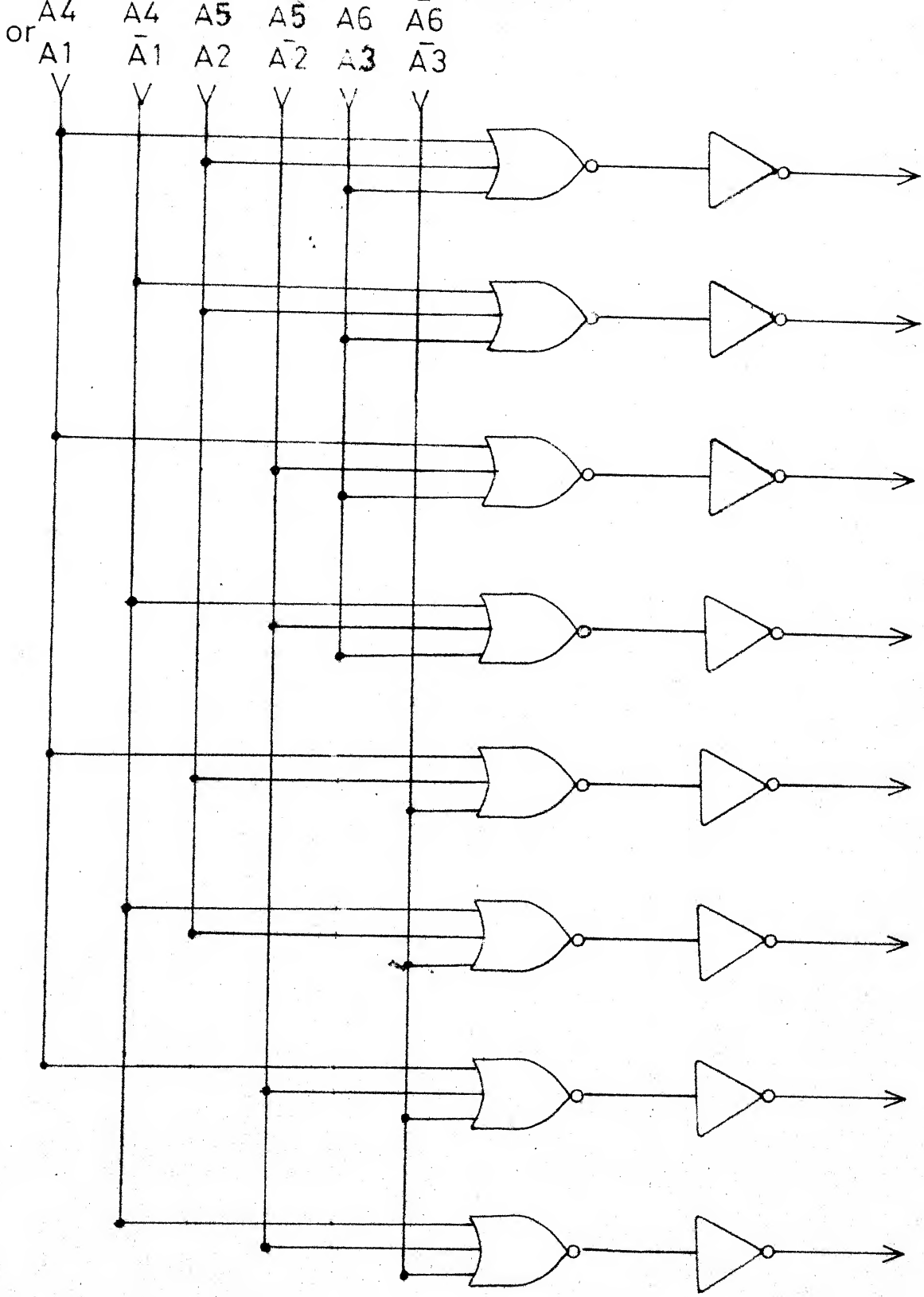


FIG. 2·5 (a) ADDRESS DECODER (1 ST STAGE)

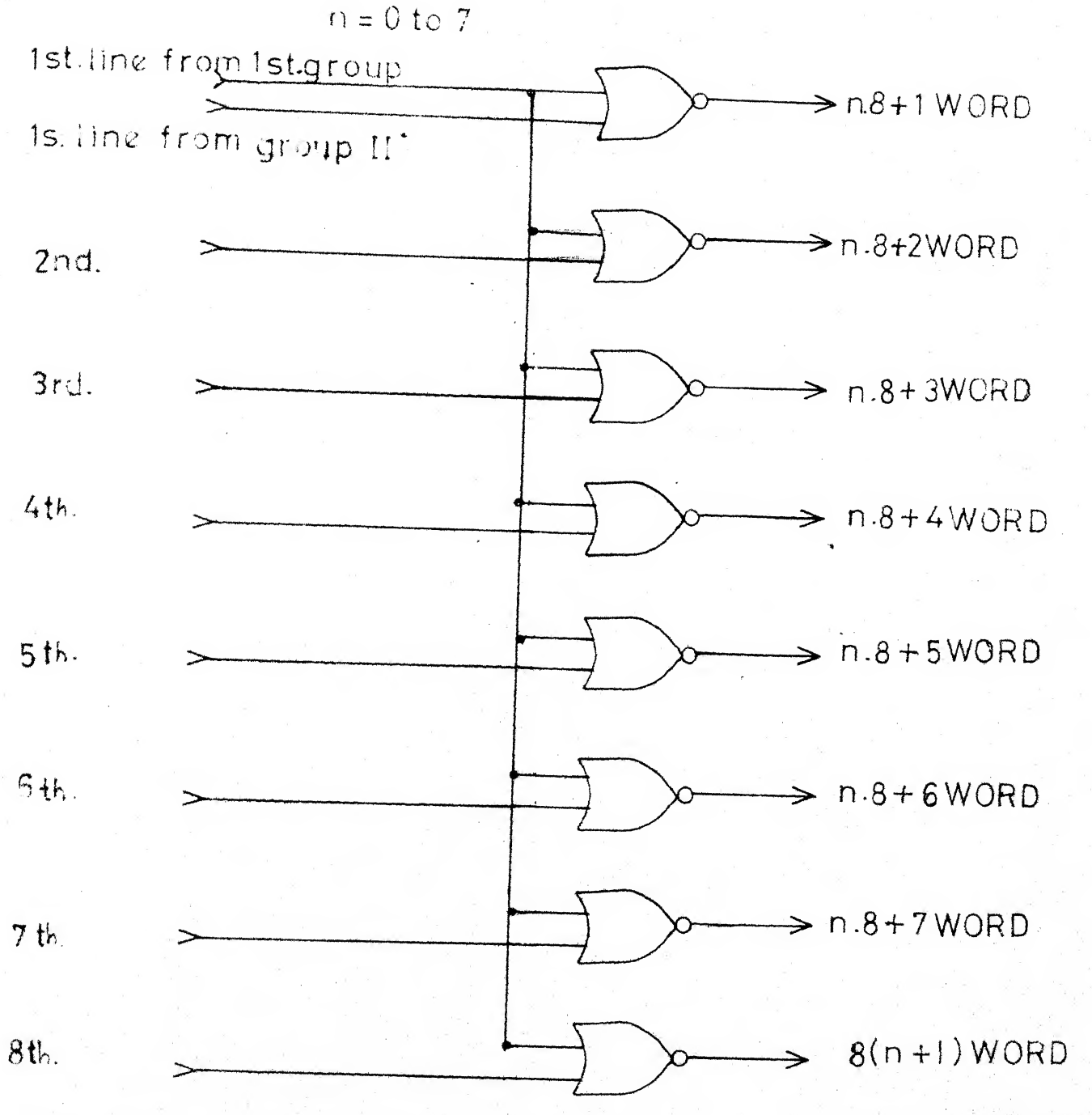


FIG 2.5(b) ADDRESS DECODER (SECOND STAGE)
EIGHT SUCH ARE REQUIRED

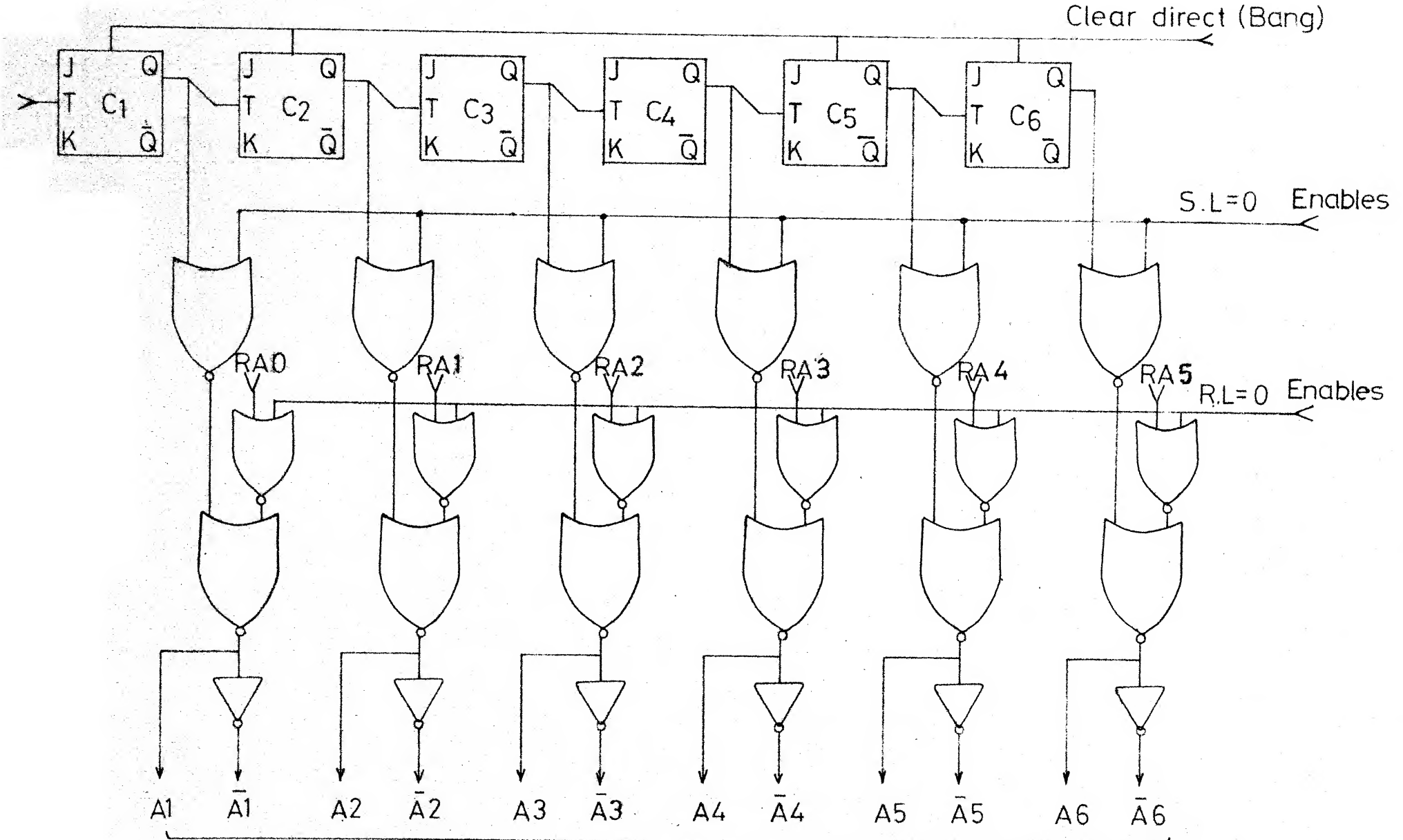


FIG. 2·6(a) COUNTER AND CONTROL LOGIC.

Address Decoder:

The address Decoder gates the date from 'Data Register' to the selected group of four 4-bit buffer register. The address of the selected group of 4-bit buffers comes from the 'Control Register' in Random Loading mode or from the 6 bit counter in the sequential loading mode. The 64 decoding tree is shown in Figure 2.5.

6 Bit Counter:

After loading of every data word into Data Register, computer sends out a 'Data Ready Pulse'. The 'Data Ready Pulse' is delayed by 'D' (0.5 to 1.5) sec microseconds and fed to the 6 bit counter. The delayed 'Data Ready Pulse' thus increments the counter to direct data words to successive groups of 4-bit Buffers. The counter is shown in the circuit diagram of control logic in Figure 2.6. The delay 'D' must be greater than the time required for loading the addressed group of 4-bit buffer registers and less than the time interval between two successive 'Data Ready Pulses'. Under a Data Channel operation the minimum time interval between two 'Data Ready Pulse' is two microseconds. Hence delay 'D' can be in between 0.5 and 1.5 microseconds.

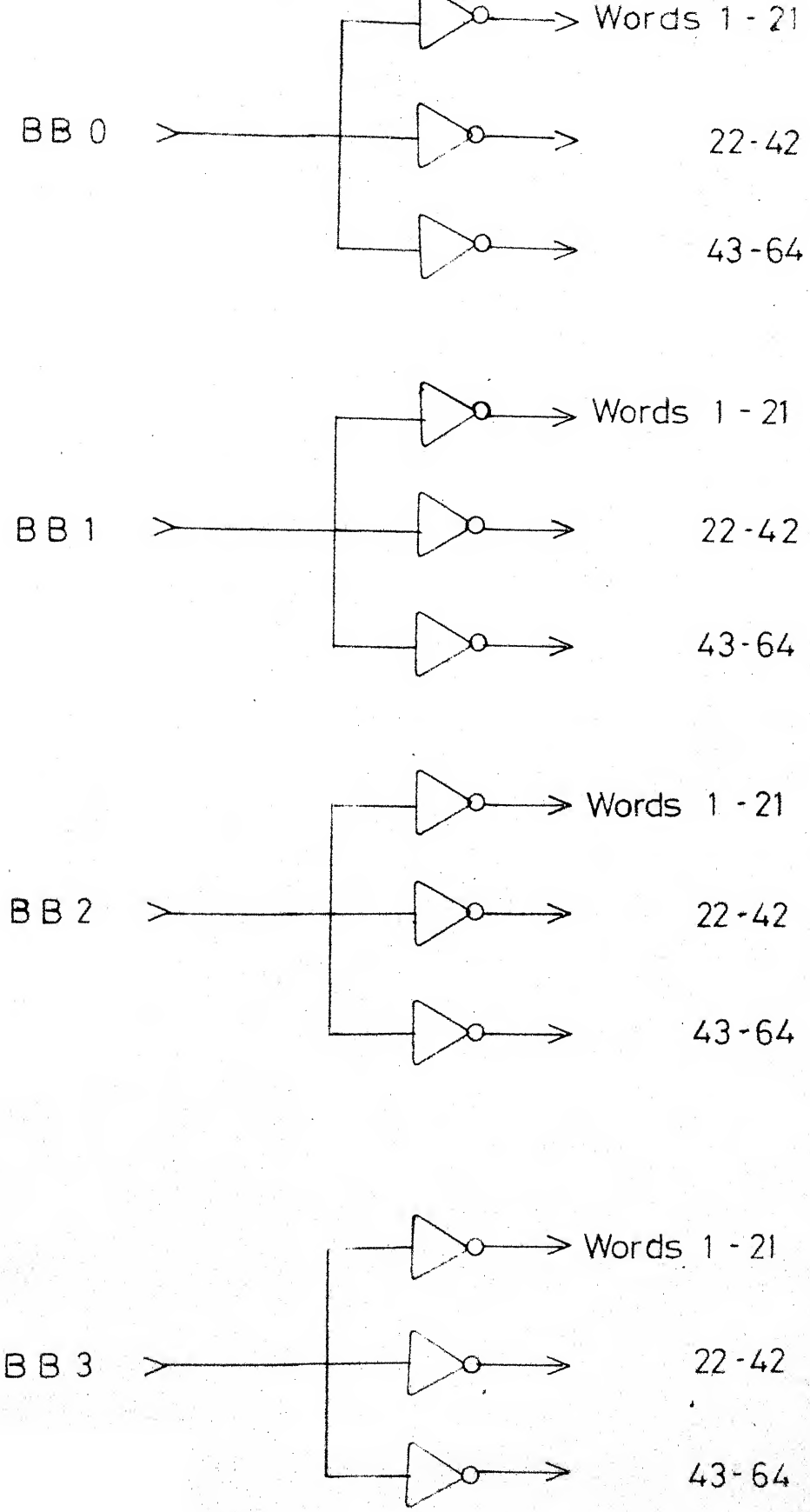


FIG. 2.7. BYTE ADDRESS BUFFERING.

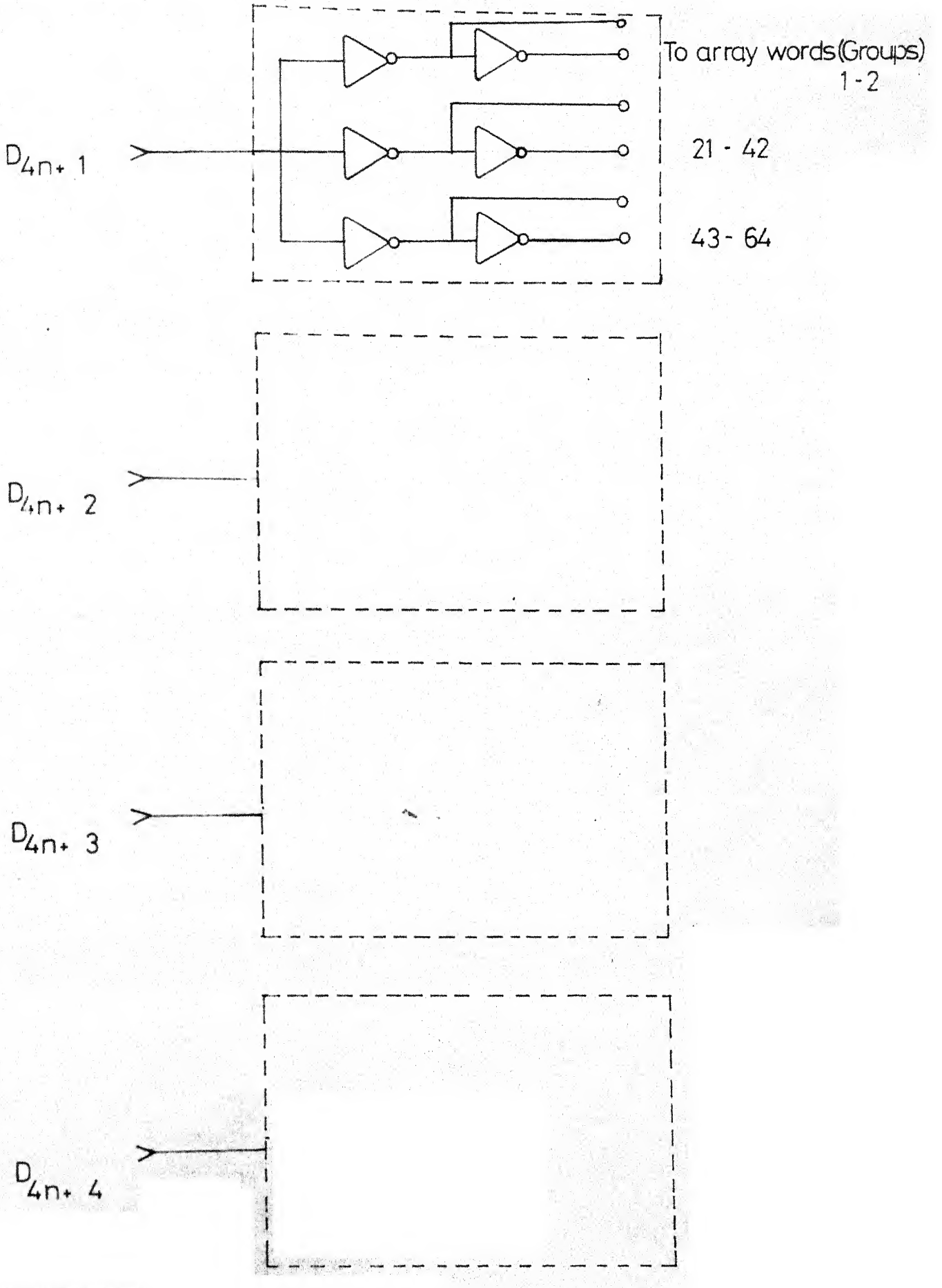
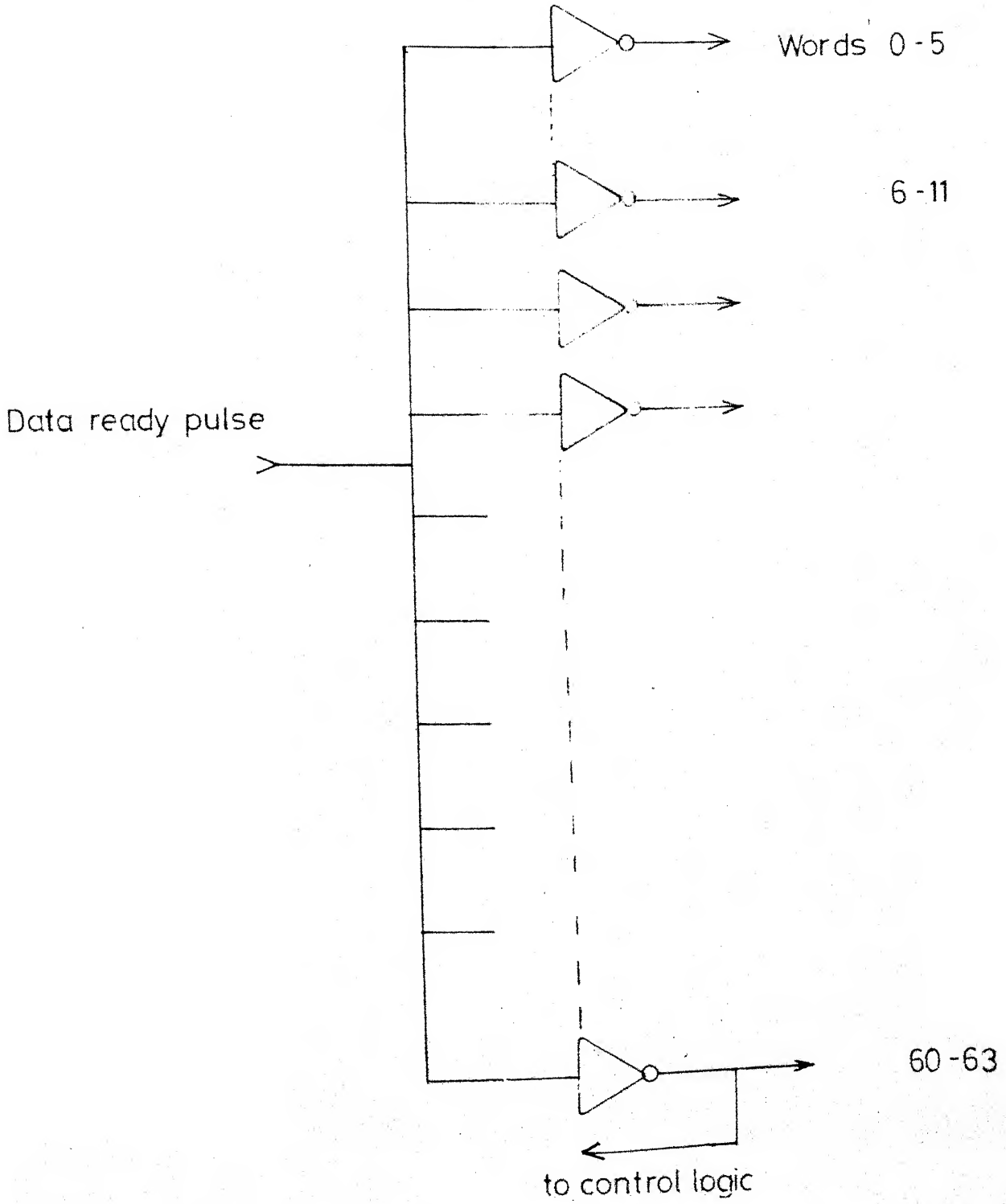


FIG.2-8.4BITS OF DATA REGISTER.



THE DATA READY PULSE GOES TO THE 256 DUAL 4 BIT SHIFT REGISTER

FIG.2.9 BUFFERING ARRANGMENT FOR DATA READY PULSE

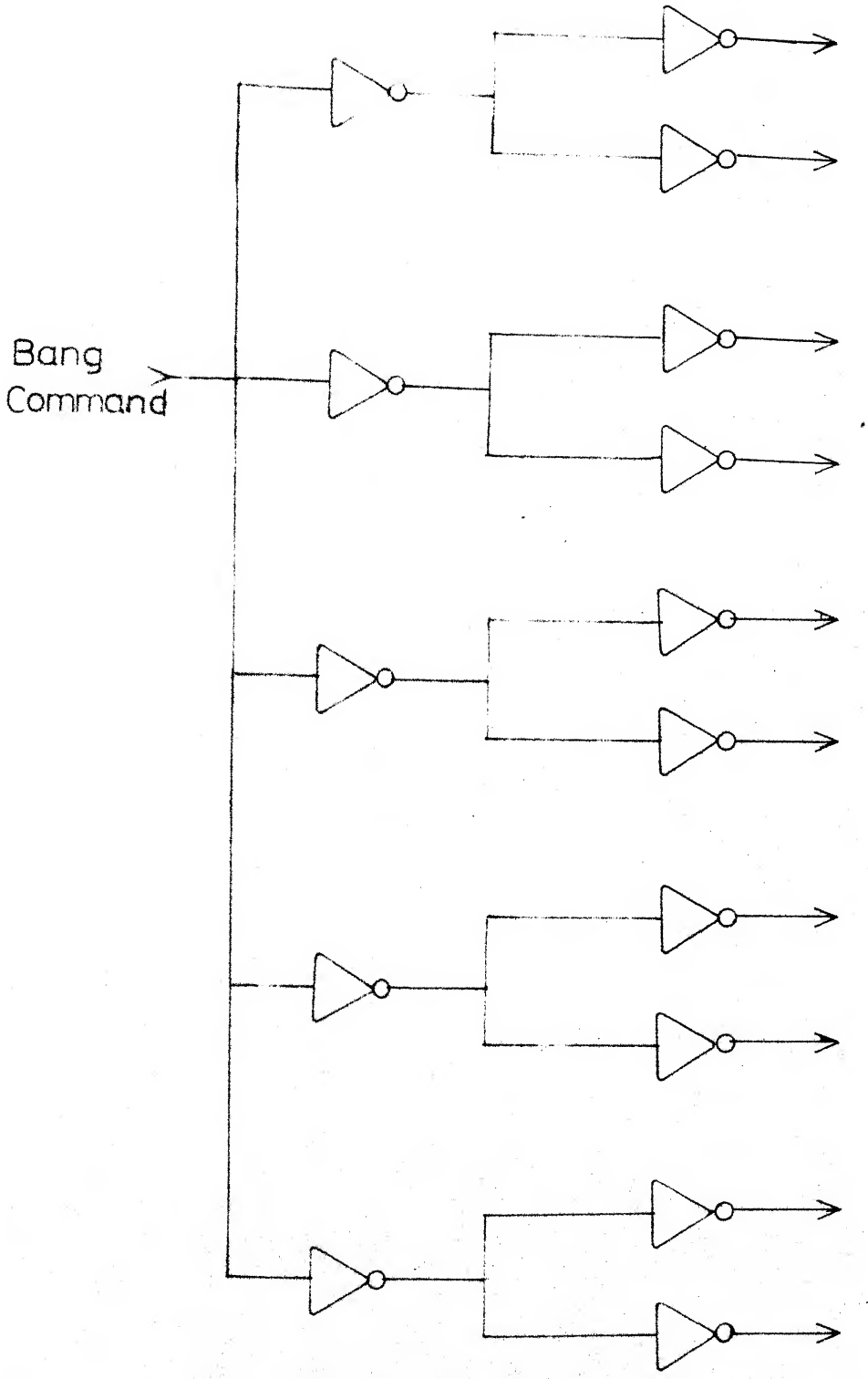


FIG. 2.10. BANG COMMAND BUFFERING. THE BANG COMMAND TO DRIVE (256 X 4) FLIP-FLOPS

Control Logic:

The 'Control Logic' executes the mode of loading as indicated in the control register. It also generates the 'Delayed Pulse' and 'Bang Command'. The inputs to the Control Logic are S.L., R.L. 'Operation Complete' bits from the 'Control Register' and 'Data Ready Pulse' from the processor controller. The logical diagram of the Control Logic is shown in Figure 2.6.

The Byte address, 'Data Register Output, 'Data Ready Pulse' and 'Bang Command' have to feed a number of circuits and so need buffering to increase fan out. The buffering scheme used for this interface is shown in Fig. 2.7, 2.8, 2.9, 2.10 respectively.

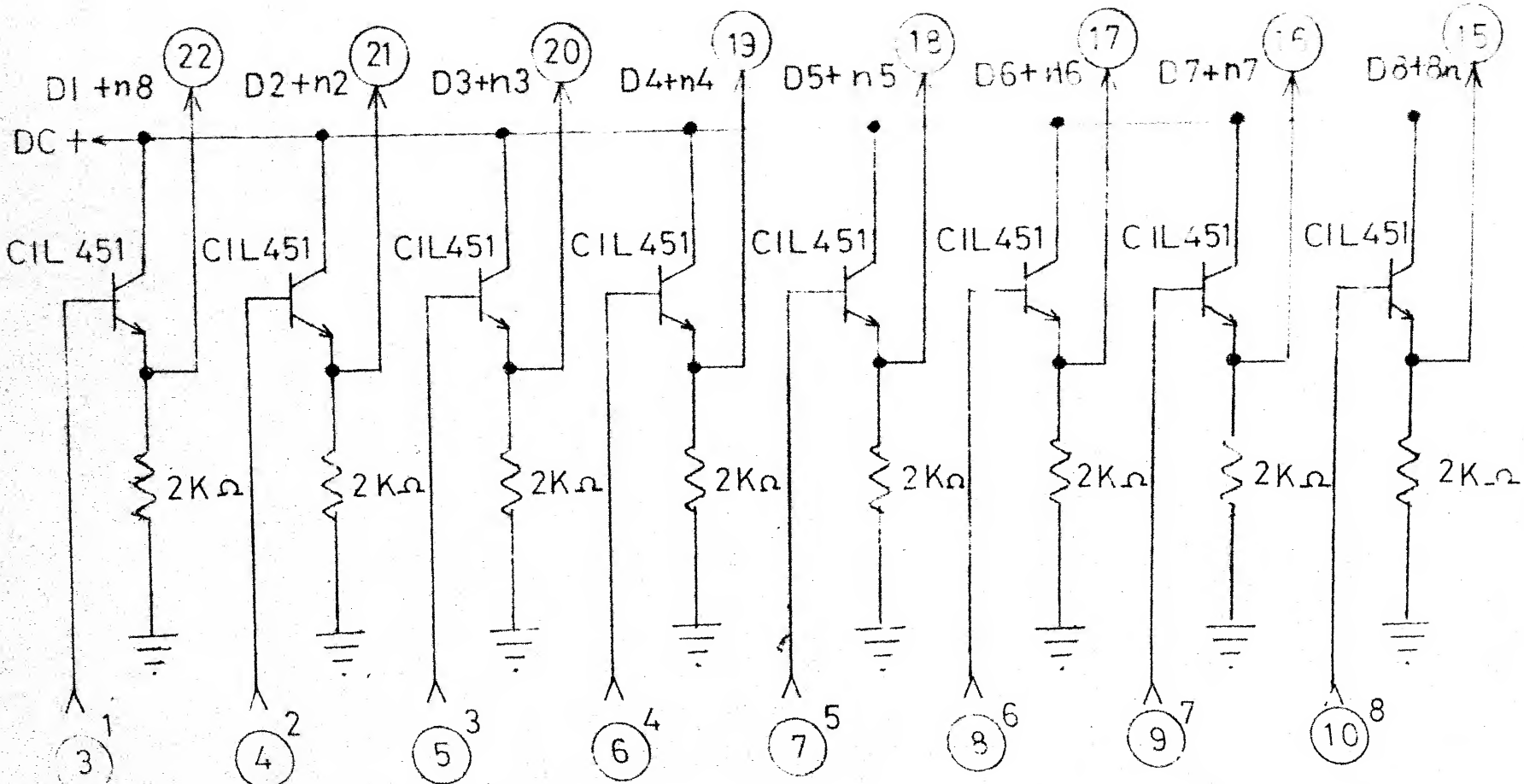


FIG. 3-1. INPUT BUFFER n = 0 To 3

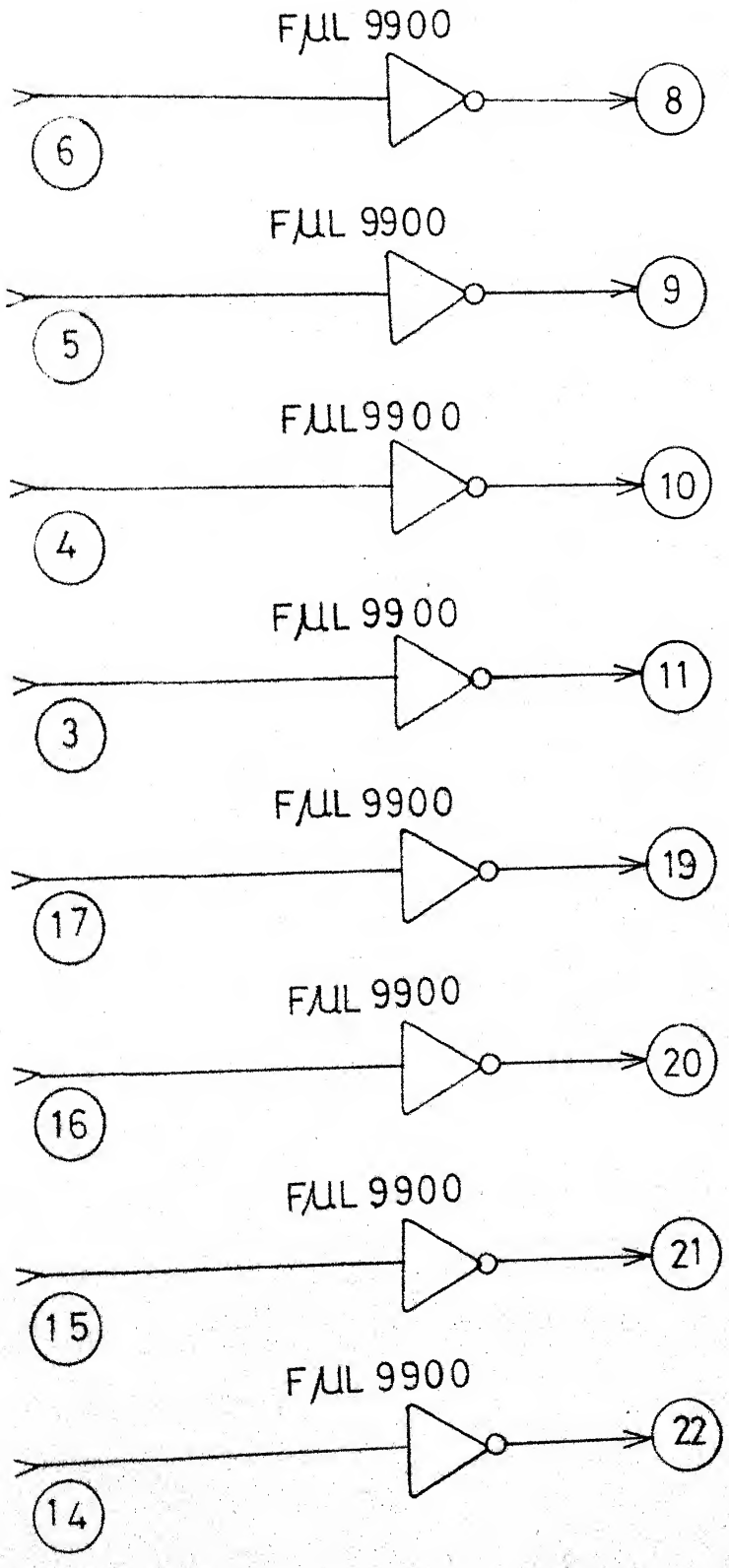


FIG. 3-2 INPUT INVERTERS

CHAPTER III

DESIGN FOR 16 ELEMENT ARRAY

Even though the system design is for a 256 element array, it was decided to implement only a 16-element array in the first phase, so it is required to design an interface for the experimental array of 16 phase shifters involving four 16-bit word transfers with four bits per phase shifter. Since IBM 1800 system does not provide digital output, the digital input points of the $D/_A$ converter are brought out.

Input Buffer:

To avoid the loading on the registers of IBM 1800, emitter followers are designed and the circuit configuration is shown in Figure 3.1. Four printed circuit boards, containing eight emitter followers each, are used.

Input Inverters:

To feed the buffer, the data bits along with their complements are required. The circuit diagram of an 'Input Inverter' is shown in Figure 3.2 . Two printed boards accomodate all the necessary buffers.

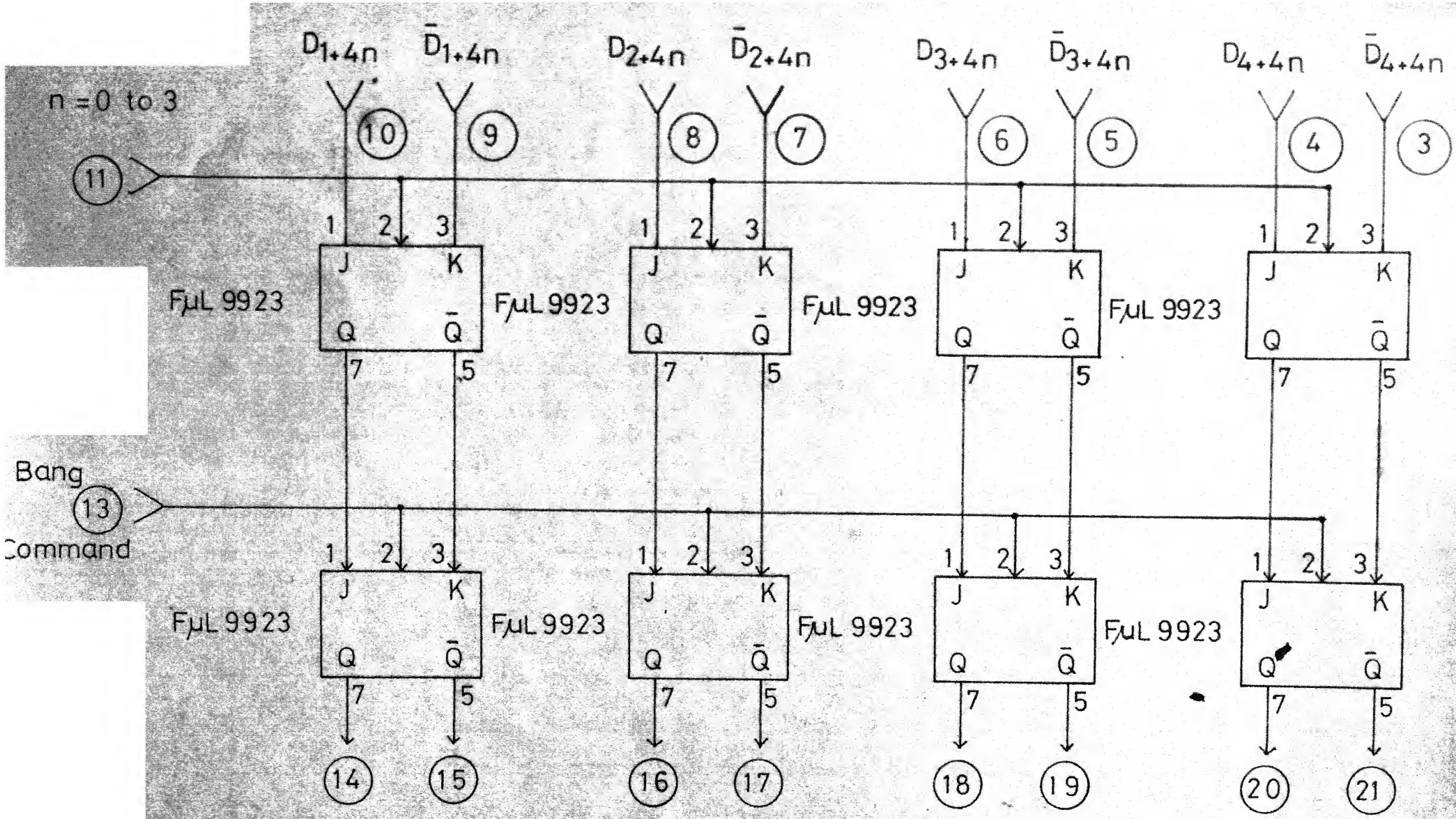


FIG. 3-3 DUAL-4 BIT SHIFT REGISTER.

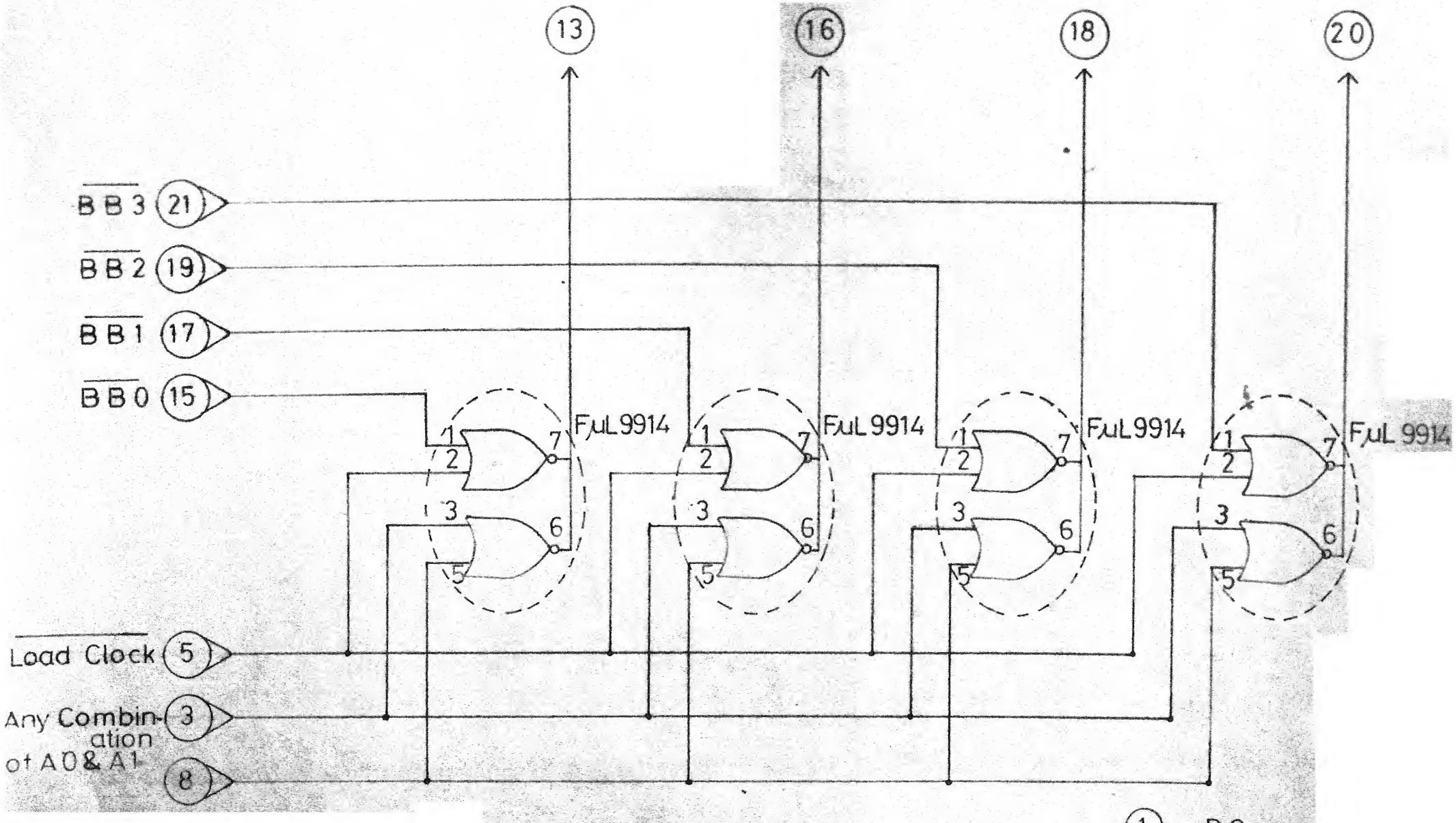


FIG. 3.4. WORD ADDRESS

Array of shift registers:

For the sixteen element array to be driven, four word transfers are required. The circuit diagram of a typical dual 4-bit shift register is shown in Figure 3.3 . The clock pulse is applied to the flip-flops in the buffer section only when the group address, Byte address and the 'Data Ready Pulse' are present. 16 printed circuit boards contain the 16 dual 4-bit shift registers.

Word address:

Since there are four word transfers two address bits are sufficient. Corresponding to the two bits, four address lines are derived. To enable data entry to a dual 4-bit Register, Byte address bit, two out of four address lines and 'Data Ready Pulse' are ended. If all the Byte address bits are 'o' (logical) then entire word can be loaded. The circuit to obtain the word address is in Figure 3.4 . Four printed circuit boards provide the addresses.

Control Logic:

As explained in Chapter-2, depending upon the status of the 'Control Register' Control Logic supervises the Data transfer. As there are only four Data Word transfers,

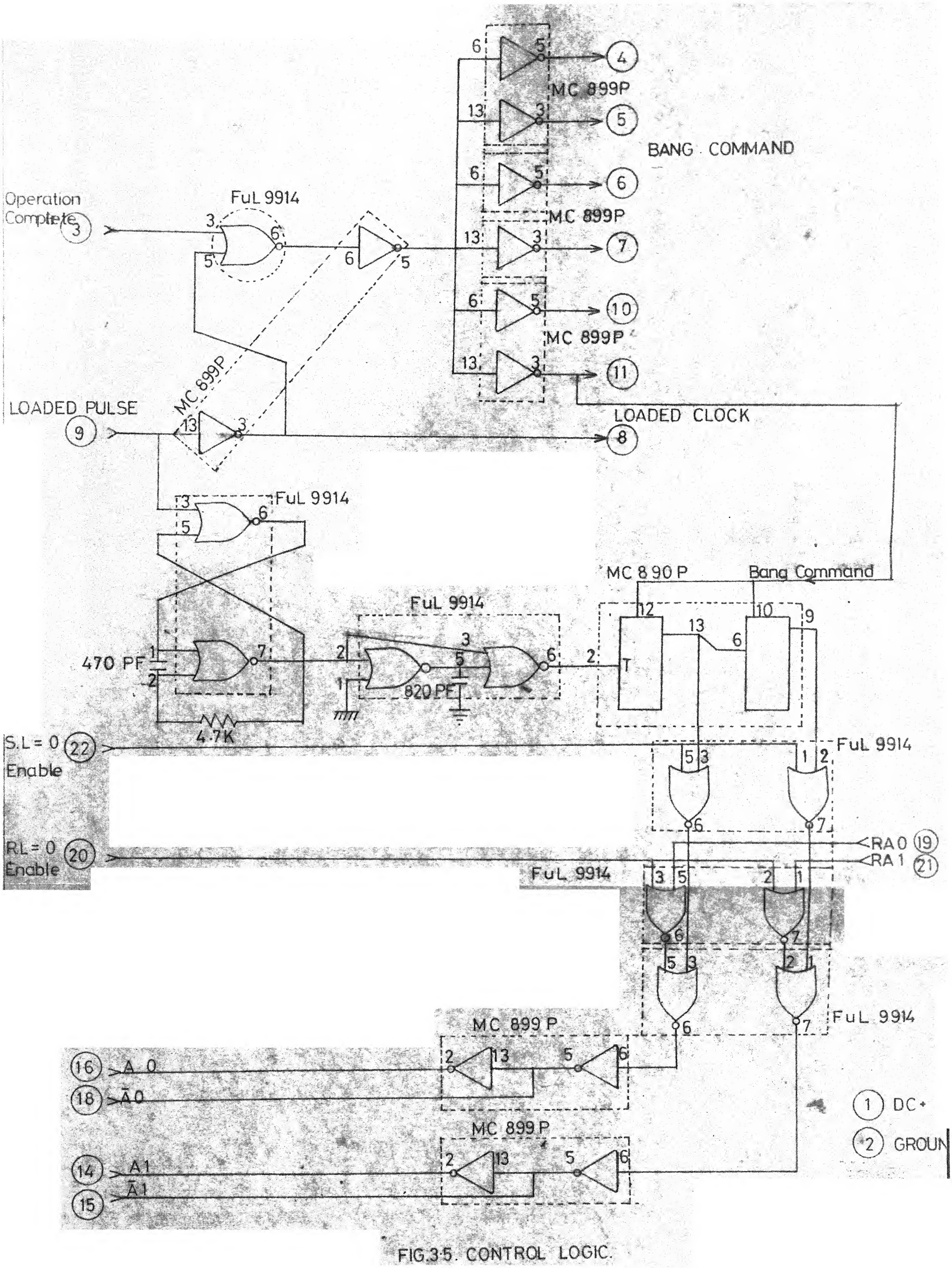


FIG.3·5. CONTROL LOGIC.

a two bit binary counter is required which is included in the Control Logic Card (Figure 3.5). When the 'operation complete' bit is turned off the 'Bang Command' is generated and as it has to feed 64 flip-flops, six buffers are used to increase the fan out. The 'Data Ready Pulse' is delayed by 5 microseconds and applied to the two bit counter. Counter output goes to the Address Decoder if S.L. bit is turned Off and R.L. bit is turned ON. Address is taken from Control Register if S.L bit is turned ON and R.I bit is turned Off. The Control Logic also consists of the circuit to select the address from the 'Control Register' or counter in accordance with conditions S.L bit turned ON. R.L bit turned Off or S.L bit turned Off R.L bit turned ON respectively.

Physical Layout of the Interface:

The interface consists of 29 printed circuit boards of $6\frac{1}{2}$" x $4\frac{1}{2}$" size which are housed in two cages mounted on 19" bud rack. The back pannel wiring of the 22-pin connectors is shown in Tables 3.1 and 3.2 . Interconnection between the cages are done by transferring the contacts with the help of extender cards. The outputs of the interface i.e. the outputs and their complements are all brought out and terminated in eight 16- pin connectors

TABLE - 3.3

16 Pin connector Number	Terminated with
1	Outputs of 'o'word 0-15 bits on 1-16 pins
2	Output complements of 'o' word "
3	Outputs of '1' word "
4	Output complements of '1' word "
5	Outputs of '2' word "
6	Output Complements of '2' word "
7	Outputs of '3' word "
8	Output complements of '3' word "
9	Output from Computer(Data Register)
10	Output from computer(Control Register)

on the front pannel. The signal interconnection between the cages and the front pannel is shown in Table 3.3 . The front pannel also contains two 16-pin connectors to accept the computer output. A regulated D.C. power supply of 3.6V, 3 amps. is mounted on the same rack.

Testing of the Interface:

Testing of the interface requires the generation of input signals and verification of the output. For this purpose a 16 bit Data pannel is designed. This contains two rows of 16 toggle switches each, one to simulate 'Data Register' and the other to simulate 'Control Register'. Each toggle switch can apply 3V logical 1 or OV logical 0. The Data Pannel also contains 16 lamp indicators (GEC display lamps) and two stage lamp drivers. The outputs of the toggle switches and the input to the indicator lamps are terminated on 16 pin connectors. Banana Sockets to externally access the indicator lamps are also provided. The lay out of the Data pannel and two stages of a lamp driver are shown in Figure 3.6 .

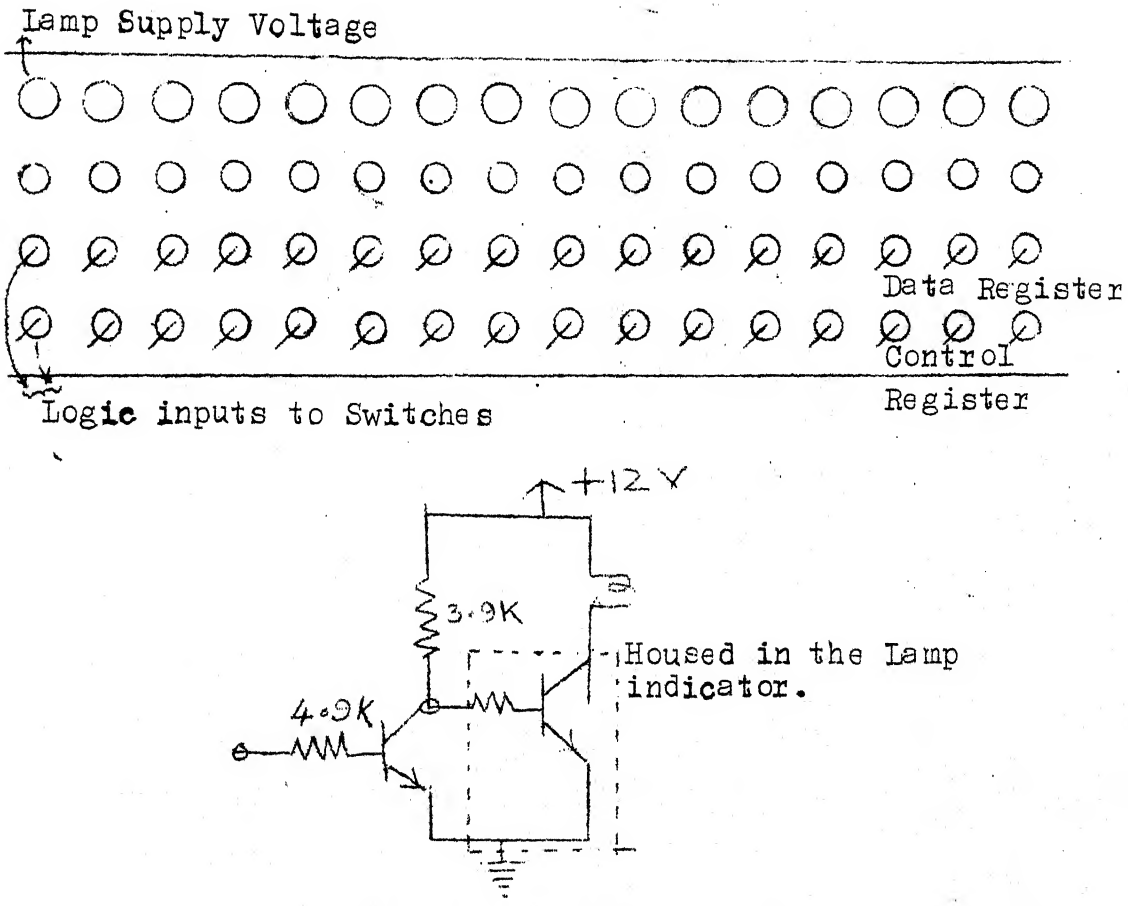


Figure 3.6 Data Pannel

The first row of toggle switches is used as 'Data Register' and the second row is used as the Control Register whose outputs are plugged into the front pannel of the interface. The data to be loaded is set in the first row of switches and the control information is set in the second row of switches.

The 'Data Ready Pulse' is obtained from the TYPE R116 programmable pulse generator, Tektronix, by operating it in the single pulse mode. For each setting of the Data and Control switches the 'Data Ready Pulse' is given twice, once with the operation complete switch in 1 state and next time in '0' state. The first pulse transfers the data into the Buffers selected and the second pulse shifts the data to the phase shifter registers.

The settings of the address switches of the 'Control Register' indicate the address of the 16 bit register* into which the information from the 'Data Register' will be loaded. In the front pannel the 16-pin connector where the outputs of the addressed 16 bit register are termined, can be identified. By connecting the lamp indicator chord to the selected 16-pin connector, the data entry into the addressed phase shifter can be tested. For different settings of the Byte address switches, the data entry into the individual Dual 4-bit shift registers is verified. Same test is repeated for different data and addresses.

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*The 16-bit Register is a group of four Dual 4-bit shift registers.

Timing Considerations:

It take 15* microseconds to load the buffer under a data channel operation and about 40 seconds in direct program control.

CHAPTER IV

CONCLUSIONS

An interface for 256 element array has been designed with RTL gates and flip-flops. Initially an interface for 16 element array is fabricated, providing scope for expansion for 256 element array. Extended Control Logic Buffers and Address Decoder circuits are required for expanding to 256 element array.

Since the appropriate hardware features on IBM 1800 were not available, the interface has been tested with the data entry through switches. Both Random, Sequential loading modes have been tested. The cables used for bringing out the outputs must be twisted pans (signal and ground) of wires.

It is expected that a working radar unit will have in the neighbourhood of one thousand points in the array . The major problems involved in designing interface for larger arrays are discussed below:

1. The need to transmit a large amount of data (1024 bits for 256 element array, 4096 bits for 1024 element array) within a short period, typically 1 millisecond (Chapter II Timing Considerations). Since we typically get

a word out of a computer in 4 microseconds, we need computer with larger number of bits per word. If we assume a speed of 4 microseconds per 16-bit word, in the one millisecond interval, during which buffers are loaded serially and then shifted into the phase shifter Registers, 250 words can be transferred from the computer to the array of Registers. With two words for control Register input and the last word for display data, only 247 words are available for Phase Commands (3952 bits). We find that data for a 1024 element array, can not be transmitted within 1 millisecond.

2. As explained in Chapter II under "Array of Element Registers' data transfer from all buffers to corresponding phase shifters is accomplished simultaneously with a single Pulse. For a 1024 element array, the buffer must provide a fan out of 4096 (RTL) load units. For the 256 element array using IC buffers about 90 chips are required. For the 1024 element array about 370 chips are required, just to increase the fan out of the 'Bang Command' . Alternatively one can achieve necessary fan out efficiently by using descrete component buffer amplifiers. It is expected that one such buffer amplifier can drive 100 circuits. It will be necessary to use fast switching transistors so that fall times will be less than 100 nanoseconds.

A similar arrangement of heavy buffering will be required for driving from the 'Data Register' for 1024 element array. Each buffer between the Data Register output and the input to 256 flip-flops, must provide a fan out of 256 load (R.T.L.) units.

3. Since all the outputs and their complements of 'Phase Shifter Registers' are to be brought out, there will be a large number of output lines (8192 lines for 1024 element array) each of which carries pulses with rise and fall times of the order of 10 to 100 microseconds (all occuring at the same time). To eliminate crosstalk, multicore flat cables* are desirable. Stage delays in RTLs which are of the order of 20 to 30 nanoseconds will not effect the performance of the interface even if a few more stage delays are added when constructing the 1024 branch decoder.

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* The flat cables used in IBM 1800 consist of 24 pairs of parallel signal and ground conductor strips insulated by plastic.

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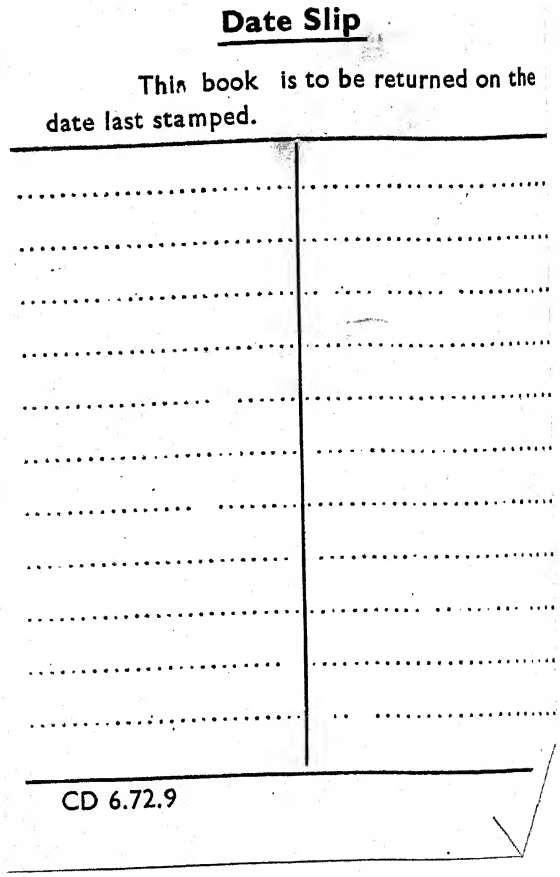

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